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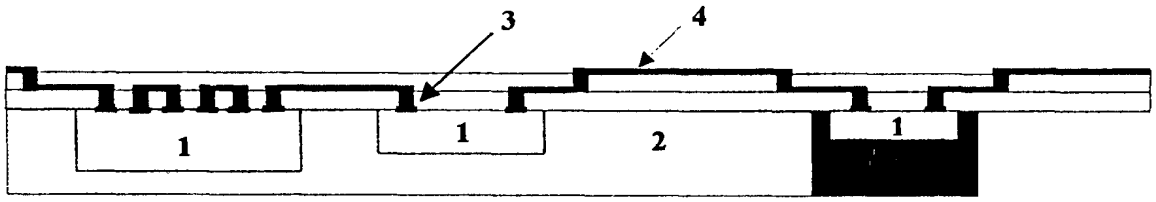

(57) Abstract

The invention relates to a fabrication method and technique for producing functional devices where active and/or passive components are embedded and interconnected during the substrate fabrication process. It is characteristic for the invention that the active and passive components are embedded into low–cost polymer substrates, preferably flexible, and interconnected using photodefinable dielectrics and the electroless copper deposition. Besides embedding passive components they can be fabricated using dielectrics and electroless deposition processes. The fabrication is carried out at ambient temperatures without vacuum–based processes like evaporation or sputtering. It is also an important advantage of the invention that wire bonding or soldering are not needed, since the latter interconnection techniques will meet increasing difficulties with higher frequencies and smaller interconnection volumes. The interconnections of active components produced with a technique according to the present invention are electrically very good and their mechanical reliability is superior to those produced with the existing techniques.

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Method for manufacturing solderless high density electronic modules

This invention relates to a manufacturing method of electronic devices which combines the solderless fabrication of reliable high density interconnections between active and passive components, packaging and manufacturing of structural substrate.

Continually increasing functionality of integrated circuits – especially higher signal transmission rates, lower operating voltages and smaller line widths in integrated circuits – imposes increasing demands on the physical and chemical compatibility between dissimilar materials in electrical contacts as well as on manufacturing technologies. Therefore, the reliability of the most advanced electronics is becoming one of the most important factors in limiting electrical performance. The reliability of electronics is especially important in portable products, because these high performance products with ever higher packaging densities experience – in addition to their operational stresses - various environments. Moreover, the usage of new environmental-friendly materials and processes set additional requirements to the reliability of electronics. On the other hand, shorter time-to-market cycles increase the reliability risk, because regardless of more effective R&D cycles especially new materials and manufacturing technologies demand careful evaluation and testing of products.

When producing ever higher density and higher performance electronic devices, more fundamental limitations are also being encountered the solutions to which will alter presently used materials and manufacturing techniques. For example, increasing I/O densities and smaller conductor widths of microcircuits require thinner metallizations and smaller interconnection volumes, and therefore higher current densities or interfacial chemical reactions between thin material layers, which are difficult to control, increase the failure risk of electronic products. Correspondingly, the increase in the wiring densities of printed circuit boards decreases the solder joint volumes, when the BGA and CSP components and especially Flip Chip assemblies are being used in greater extent. Hence, harmful effects of relative large fractions of brittle intermetallic compounds and impurities become stronger in the microjoints being under larger shear strains; the fact that decreases the reliability significantly.

"Flip Chip (FC)" technique, in which bare, non-encapsulated semiconductor chips are interconnected directly onto substrate, resembles BGA and CSP techniques, where interconnection bumps generally made of SnPb solder alloy are also under component. However,

microcircuit is not encapsulated and the bump pitch is smaller – typically below 250 μm. Due to the smallness of bumps the accuracy of assembly machines must be very high regardless of the self alignment effect of molten solder balls. For the same reason underfill material is always used to protect the microcircuit, when the substrate material is FR4 or comparable. In addition to diminishing the stress peaks, the underfill protects the microcircuit from harmful effects of moisture and contaminations. The underfilling requires, however, additional process steps and thereby increases processing costs. Besides perfect underfilling becomes ever more difficult with smaller solder bumps and increasing bump densities. The testing and repair must be carried out before the underfilling, because after the cure of the underfill the microcircuit cannot be removed from the substrate. Flip chip assembly requires also high quality printed wiring boards.

With increased interconnection densities both bare and encapsulated semiconductor chips are getting closer to the substrate surface, which adds to shear strains and so increases the failure risk of a component board assembled with surface mount technology. The situation is also especially problematic due to low metallurgical stability of very small solder joints and large mismatch between the coefficients of thermal expansion of the substrate and silicon. Despite the underfilling the solder joints may crack during testing.

One of the most significant obstacles to the adoption of CSP packages and Flip Chip technique is the availability of low-cost and high density printed wiring boards. Presently so-called additive printed wiring board manufacturing technologies are most promising, although they are relatively expensive. However, these technologies offer significant advantages in improving the reliability of microjoints as well as in embedding passive and active components. It is expected that the line widths of integrated circuits will decrease well below 0.1 μm before the year 2010. Correspondingly, the contact areas or (I/O)'s pads on the chip will decrease below 10 μm, when the number of interconnections increases and interconnection volumes decrease strongly. In such a situation the attention will be paid to the metallurgical stability of small solder joints and to the fabrication of printed wiring boards, because the production of contact areas of 10 μm in order of magnitude sets very high requirements for the development of printed wiring board technology.

New environmental regulations and consumers' increasing awareness of environment issues drive electronics manufacturing towards lead-free and no-clean solutions. Therefore, new materials and manufacturing technologies are adopted, which may affect also the reliability of electronics. Lead is a harmful element to human beings and therefore the use of lead is banned or

restricted in many applications. The electronics industry is employing lead above all in solder alloys and in protective coatings on components and printed wiring boards.

Presently there is no drop-in replacement for the eutectic tin-lead solder alloys in electronics manufacturing, although some very promising alternatives have been developed. Lead-free solders having the best mechanical properties are tin-rich alloys which have small amounts of alloying elements. Therefore their melting points are 30-50 °C higher than those of the most common tin-lead solders, that will change also the component assembly processes. Likewise, the usage of lead-free surface finishes on printed wiring boards will change the assembly processes. Along with the lead-free issue much attention is being paid to the environmental causes of fluxes and other chemicals used in soldering. Surface mount technology being based on so-called no-clean soldering is very much alike to conventional surface mount technology except for the cleaning of flux residues. The development of no-clean processes is also driven by the expectations of lower production costs. The removal of the cleaning process from the production line reduces equipment, chemical, labor and waste disposal costs. This is, however, possible only if the no-clean assembly process can be executed reliably.

Hence, the need to enhance concurrently the reliability, performance and economy of electronics manufacturing drives the integration of manufacturing technologies. Similarly, continuously decreasing size and increasing number of passive components on the printed wiring board drives to integrate the components into the substrate. Especially manufacturers of consumer electronics are interested in integration of passive components into the substrate. In this way more space is left for other discrete components. In addition to the increased packaging density, i.e. larger silicon-to-substrate ration, the manufacturing process is simplified. But also active components can be embedded into printed wiring boards.

Integration of microcircuits into printed wiring board with so-called "chip first"-technique is one of the methods to solve the problems related to interconnecting high density microcircuits. In this method a microcircuit is connected to the substrate before the wiring and electrical contacts are formed.

The patents US 5353195, US 5353498, US 5422513 and US 5497033 present solutions to problems related to high density component interconnections.

In the methods presented in these patents the microcircuits are attached to ceramic or polymeric substrates. When microcircuits are integrated into the ceramic substrate, cavities being slightly larger than the microcircuits are formed so that the top surfaces of the microcircuits are on the same level with the ceramic substrate. The cavities can be formed by mechanical or laser drilling or by casting the substrate into a mould. Microcircuits are attached to the cavities with an adhesive from the backside of the circuits, after which the gap between the microcircuits and the substrate is cast with a ceramic or polymer material. After this a polyimide film is laminated onto the substrate surface and the vias to the microcircuits are formed through the polyimide film by laser drilling. The wiring is produced with the semiadditive technique, in which the surface of the substrate is sputtered with a metal or alloy, and this is followed by the electrochemical plating of the conductors. Because of the nonplanarity of the substrate surface the exposure of the photoimageable resist is made with laser. When microcircuits are integrated into polymeric substrate, the microcircuits are aligned onto a thin polymer film. This is followed by casting of the microcircuits into the epoxy by using a casting mould. The properties of the epoxy are improved by filling the polymer with glass or ceramic particles, mostly with silica particles. The epoxy must have good mechanical durability, low shrinkage, similar CTE with silicon, and it must be compatible also with other materials used. After casting the component is detached from the mold and the vias are formed through the thin polymer film with the laser drilling. The wiring structure on the component surface is also produced with the semiadditive technique.

According to the above-mentioned patents the manufacturing of electrical contacts to the microcircuits and the wiring on the substrate requires the field metallisation which is produced by sputtering before the electrolytic plating. The sputtering technique demands the use of vacuum, which makes the process time-consuming, expensive and restricts the size of the substrate. Moreover, the perfect coverage of the complicated surfaces is difficult and in some applications it requires the use of elevated temperatures. In mass production the repeated use of vacuum decreases the throughput of the process. The size of the vacuum chamber restricts the size and number of the substrates to be sputtered simultaneously. The semiadditive method requires the coating of several thin metal layers (for example, adhesion layers). Consequently, there are several interfaces between dissimilar metallisations which present potential reliability risk. In the semiadditive manufacturing of the wiring structure the excess panel plating is etched away. The etching process sets limitations to the minimum line width which can be fabricated. It also produces toxic wastes.

The principal objective of the present invention related to manufacturing reliable high density electronics is to provide a new technique and method without the drawbacks of the techniques and methods of the known art. The interconnections and microjoints manufactured by using the technique and method of the present invention are electrically, mechanically and chemically superior to those produced with the techniques of the known art. Passive components that are connected to active components can be fabricated by using the technique of the present invention.

In the following the embodiments of the present invention and its benefits in comparison to the fabrication techniques of the previous art are described.

The fully additive fabrication technique of the present invention is simpler to execute, it is more cost-effective and it can be used to eliminate the disadvantages related to the techniques of the known art. With the technique and method of the present invention a package of one active component or integrated functional modules with one or several active and passive components can be fabricated. Microcircuits of various thickness can be embedded into a single module board so that the active surface of the components are at the same level with the substrate. Copper, nickel or gold can be used as a pad metallisation for the embedded microcircuits. When copper (I/O) pads on integrated circuits are used copper-to-copper interconnections can be fabricated with the invented fully additive active component embedding and interconnection technique. In such a case the interconnections are made solely of copper.

More specifically the present invention concerning the solderless fabrication technique and method are characterised by what is stated in the novelty parts of the claims.

Several advantages are achieved with the fully additive active component embedding technique as compared the techniques of the known art. The fully additive active component embedding technique does not require metal etching at any process step. The interconnections are fabricated at ambient temperatures using wet-chemical, electroless deposition process. The composition of the electroless baths can be refreshed during the deposition process, thus enabling a long service life and producing only a small amount of bath residuals. The fully additive embedding technique of microcircuits includes only a few process steps. Therefore, the technique is reliable, cost-effective and simple to use. Both single large area components and several small area components can be interconnected simultaneously with the technique. Copper conductors and

copper-to-copper electrical contacts can be fabricated with the invented technique. Consequently, there is the perfect metallurgical compatibility between contact metals and therefore the problems related to small interconnections produced with the techniques of the known art can be eliminated. The fabrication process does not require vacuum or high processing temperatures during the fabrication of the interconnections. As a matter of fact, the technique and method of the present invention combines the three presently separate manufacturing processes: substrate or PWB manufacturing, active component packaging and the fabrication of the interconnections into one simple, reliable and cost-effective fabrication process. Because the electrical interconnections are fabricated using chemical deposition, soldering is not needed. This gives significant benefits when manufacturing reliable electrically functional high density interconnections .

Figure 1 shows schematically an integrated module board fabricated with the technique of the present invention. This example presents the cross-section of a "printed wiring board" or module board containing three interconnection levels. The active components (1) are embedded into the substrate (2) so that the opening of the active components (3) are visible. The conductors for the active components openings (4) are fabricated using the fully additive build-up technique of the present invention.

In the following a simple example of integrated module boards which can be fabricated with the invented fully additive component embedding and interconnection technique is presented:

Phase 1

The microcircuits or active components (1) are embedded into a substrate (2) so that the open (I/O) pads of the components (3) are visible, while the rest of the active components are molded inside polymer substrate.

Phase 2

The flat surface of polymer is normally roughened prior to the activation step. Depending on the properties of the polymer the roughening can be made by employing chemical, mechanical, electrical or thermal treatments. The surface is roughened for achieving adequate adhesion of the deposited metal to the polymer. The roughened substrate surface and the openings or (I/O) pads of microcircuits are activated. The activation is carried out with a catalyst. Typically colloidal tin-palladium solution is used as a catalyst for the electroless copper solution. Palladium is the

catalyst for the oxidation/reduction reaction and the tin protects the palladium from the oxidation. The activated surface is electrically non-conductive.

Phase 3

The conductor structure is defined by using a permanent photodefinable polymer dielectric in the photolithographic process. Typically the photolithographic process is divided into the four processing steps: coating, exposure, development and the curing. During the exposure step the properties of the photodefinable polymer are modified so that the polymer can be dissolved selectively. During the development step the activated surface (2) is uncovered under the photodefinable polymer for the electroless copper deposition in the phase 4.

Phase 4

Electroless copper is deposited on the uncovered areas of the substrate and on the I/O's of the microcircuit. After the complex chemical reactions the copper ions are deposited onto the activated surface. The copper deposition process is autocatalytic (or self-catalytic).

Electroless copper deposition is slower than that of the electrochemical copper. The deposition rates for electroless copper are typically 2-3 μm per hour, which makes it easy to control the deposited copper thickness. The deposition rate can be adjusted with the deposition temperature, which is typically somewhat higher than room temperature. The conductivity of the copper can be increased with the increasing thickness.

The above-described fabrication steps or phases 2 – 4 are repeated several times for fabricating a desired multilayer structure with all the electrical interconnections. (In Fig. 1. the phases are repeated three times)

In addition to the above-described fabrication process, all its variations where alternative chemicals and different conductor metals than copper are used for fabricating integrated multilayer module boards belong to the scope of the present invention.

Claims

1. Manufacturing process for electrically functional devices or modules, where the contact areas of microcircuits are interconnected using lithographic processes and semiadditive build-up techniques, wherein the fabrication method and technique comprises that embedded microcircuits and passive components are processed and interconnected solderlessly into electrically functional devices or modules with the fully additive build-up substrate fabrication technique.

2. A fabrication method according to claim 1 wherein the fabrication process is comprised of the following steps:
   - Phase 1: One or several microcircuits are embedded into substrates so that the electrical contact areas of the components remains visible;
   - Phase 2: The surfaces of roughened substrates and the contact pads of the microcircuits or passives are activated;
   - Phase 3: Conductor patterns on the activated surfaces are fabricated using the photo-lithographic processing;
   - Phase 4: Concurrent fabrication of conductors and interconnections using the electroless copper deposition.

3. A technique according to one of the claims 1 - 2 wherein the electrical interconnections of bumped or bumpless active or passive components are fabricated at ambient temperatures and under atmospheric pressure.

4. A technique according to one of the claims 1 - 3 wherein the fabrication of conductors and their interconnections do not require metal etching.

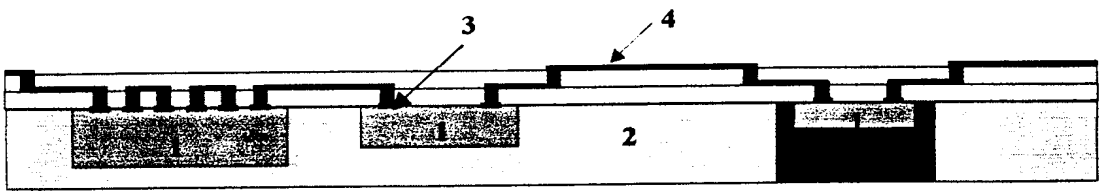

Fig. 1

INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H05K 3/02, H01L 23/52, C23C 18/16
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H05K, H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y		2
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[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 5719749 A (J.J. STOPPERAN), 17 February 1998 (17.02.98), column 1, line 7 - column 3, line 17	1-4
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/FI 00/00327

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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